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Description

INTEGRATION OF HIGH PERFORMANCE COPPER INDUCTORS WITH BOND PADS

Background of Invention

[0001] The present invention relates generally to integration of high performance copper (Cu) inductors with bond pads, and more particularly pertains to integration of high performance copper inductors with global interconnects, and with either Al bond pads or Cu bond pads, where the Cu for the inductor and the global interconnects is defined by a resist pattern above the chip passivation layer. In addition, the inductor can be fabricated by superposing the adjacent wiring layers or levels to form a laminate inductor, with the metal levels being interconnected by a bar via.

[0002] Copper inductors are being used increasingly in RF integrated circuits. The performance of a Cu inductor is maximized by maximizing the thickness of the Cu. This can be achieved by plating a thick Cu layer (>5 um) inside a re-

sist mask.

[0003] Unfortunately, it is difficult to passivate thick Cu inductors, wherein passivation serves as a diffusion barrier to protect Cu from corrosion. If the Cu inductor is formed below the last metal level (i.e. the last metal layer before the chip passivation layer), then planarization of subsequent metal levels is difficult and/or expensive. If the Cu inductor is formed at or above the last metal level, then passivation of the Cu is difficult. Typically, the last metal layer is passivated with Si3N4 and SiO2 layers, which are deposited by chemical vapor deposition (CVD), to prevent contaminants from diffusing into the transistors and wiring in the chip. However, the conformality of CVD films is not adequate to passivate thick Cu inductors. In addition, the processes used to form the inductor and the inductor passivation must not damage the bond pads.

Summary of Invention

[0004] The present invention provides integration of high performance copper inductors with global interconnects, and with either Al bond pads or Cu bond pads, where the Cu for the inductor and the global interconnects is defined by a resist pattern above the chip passivation layer. In addition, the inductor can be fabricated by superposing the

metal layer above the passivation with underlying metal wiring layers or levels to form a laminate inductor, with the metal levels being interconnected by a bar via, and having the same spiral shape as the spiral metal inductors at each metal level in the inductor stack.

[0005] The present invention provides a method for passivating thick Cu inductors separately from the chip passivation. In addition, the present invention provides methods for integrating thick inductors with bond pads, terminals and interconnect wiring using the metal layer above the chip passivation.

[0006] The subject invention uses dielectric deposition, spacer formation, and/or selective deposition of a passivating metal such as CoWP, to passivate a Cu inductor that is formed after the last metal layer. In addition, the process is integrated with the formation of bond pads, terminals and interconnect wires.

[0007] The advantages of the present invention include:

[0008] the ability to use high performance Cu inductors with minimal additional processing;

[0009] the formation of passivation over Cu inductors formed after the last metal layer;

[0010] the Cu used for the inductors can also be used as a last

metal + 1 wiring layer or for raised bond pads and for interconnect wiring;

[0011] process is compatible with raised Al bond pads or recessed Cu bond pads.

Brief Description of Drawings

[0012] The foregoing objects and advantages of the present invention for integration of high performance copper inductors with bond pads may be more readily understood by one skilled in the art with reference being had to the following detailed description of several embodiments thereof, taken in conjunction with the accompanying drawings wherein like elements are designated by identical reference numerals throughout the several views, and in which:

[0013] Figure 1 illustrates a top plan view of a first embodiment of the present invention for a spiral Cu inductor having a raised Al bond pad.

[0014] Figures 1a-1h illustrate the sequential steps a-h for fabrication of the first embodiment of the present invention for a spiral Cu inductor having a raised Al bond pad.

[0015] Figure 1a illustrates the structure after formation of last metal layer damascene Cu interconnects in an FSG dielectric using conventional processing steps.

[0016] Figure 1b illustrates the structure after depositing two layers of Si_3N_4 and an intermediate layer of SiO_2 passivation.

[0017] Figure 1c illustrates the structure after patterning of terminal vias by lithography and RIE.

[0018] Figure 1d illustrates the structure after depositing multiple layers of metal for a bond pad by PVD or CVD, depositing a Si_3N_4 layer by CVD, patterning by lithography and RIE, and depositing a Cu seed layer by PVD.

[0019] Figure 1e illustrates the structure after depositing and patterning resist for Cu inductors and depositing Cu.

[0020] Figure 1f illustrates the structure after stripping of the resist, etching Cu seed and TaN, and selectively depositing CoWP on Cu inductors.

[0021] Figure 1g illustrates the structure after coating the substrate with polyimide and forming openings to bond pads.

[0022] Figure 1h illustrates the structure after etching SiN layer on bond pads, depositing a BLM barrier, and forming C4 solder balls.

[0023] Figure 2 illustrates a top plan view of a second embodiment of the present invention for a spiral Cu inductor which is similar to the spiral Cu inductor of Figure 1 but having a recessed Cu bond pad.

[0024] Figure 2d illustrates the structure after depositing TaN barrier by PVD, and depositing Cu seed layer by PVD.

[0025] Figure e illustrates the structure after depositing and patterning resist for Cu inductors and depositing Cu by electroplating to selectively form Cu in inductor regions.

[0026]

[0027] Figure 2f illustrates the structure after stripping of the resist, etching the Cu seed and TaN barrier and selectively depositing CoWP on Cu inductors and terminals using electroless deposition.

[0028] Figure 2g illustrates the structure after coating the substrate with polyimide and forming via openings to bond pads.

[0029] Figure 2h illustrates the structure after depositing barrier layer metallurgy BLM and forming C4 solder balls.

[0030] Figure 3 illustrates a top plan view of a third embodiment of the present invention for a spiral Cu inductor having a raised Cu bond pad.

[0031] Figure 3e illustrates the structure after depositing and patterning resist for raised bond pads, Cu inductors and interconnect wiring, and depositing Cu by electroplating.

[0032] Figure 3f illustrates the structure after stripping of the resist, etching the TaN barrier, and selectively depositing

CoWP on Cu inductors, terminals and interconnect wiring using electroless deposition.

[0033] Figure 3g illustrates the structure after coating the substrate with polyimide and forming via openings to bond pads.

[0034] Figure 3h illustrates the structure after etching SiN, depositing barrier layer metallurgy BLM and forming C4 solder balls.

[0035] Figures 4a-4c, 5a-5e and 6a-6e illustrate respective first (1), second (2) and third (3) options for patterning Cu.

[0036] Figures 4a-4c illustrate option 1 in which the seed layer is deposited before the resist, followed by selective deposition of Cu.

[0037] Figure 4a illustrates, after the terminal via etch, the structure formed by depositing a TaN barrier by PVD and depositing Cu seed layer by PVD.

[0038] Figure 4b illustrates the structure formed by depositing and patterning resist for inductors, terminals and interconnects, and depositing Cu by electroplating to selectively form Cu in inductor, terminal and interconnect regions.

[0039] Figure 4c illustrates the structure after stripping resist and etching the Cu seed and barrier.

[0040] Figures 5a-5e illustrate option 2 in which the Cu seed layer is deposited after the resist, followed by blanket deposition of Cu and CMP.

[0041] Figure 5a illustrates, after the terminal via etch, the structure formed by depositing TaN barrier by PVD.

[0042]

[0043] Figure b illustrates the structure formed after depositing and patterning resist for inductors, terminals, interconnects, and depositing Cu seed layer by PVD.

[0044] Figure 5c illustrates the structure after depositing Cu by electroplating.

[0045] Figure 5d illustrates the structure after removing excess Cu by CMP or electropolishing.

[0046] Figure 5e illustrates the structure after stripping the resist and etching.

[0047] Figures 6a-6e illustrate option 3 for patterning Cu in which the barrier and seed layers are deposited after the resist and a blanket deposition of Ta and Cu, followed by CMP or etching.

[0048] Figure 6a illustrates the structure formed after terminal via patterning.

[0049] Figure 6b illustrates the structure formed after depositing and patterning resist for inductors, terminals and inter-

connects, depositing Ta adhesion layer, depositing Cu seed layer by PVD.

[0050] Figure 6c illustrates the structure after depositing Cu by electroplating to selectively form Cu in unmasked regions.

[0051] Figure 6d illustrates the structure after removing excess Cu by CMP or electropolishing, and removing TaN adhesion layer by CMP or wet etch.

[0052] Figure 6e illustrates the structure after stripping the resist and etching TaN.

[0053] Figures 7a-7d illustrate options for passivation.

[0054] Figure 7a illustrates passivation by selective metal only.

[0055] Figure 7b illustrates passivation by dielectric deposition only.

[0056] Figure 7c illustrates passivation by selective metal and dielectric deposition, which is a combination of Figures 7a and 7b.

[0057] Figure d illustrates passivation by spacer (metal or insulator), and dielectric deposition.

[0058] Figure 7e illustrates passivation by spacer (metal or insulator), and selective metal, and dielectric deposition.

[0059] Figure 7f illustrates passivation by selective metal, and spacer (metal or insulator), and dielectric deposition.

Detailed Description

[0060] Figure 1 illustrates a top plan view of a first embodiment of the present invention for a spiral Cu inductor 10 having an Al (aluminum) bond pad 12, a Cu wire terminal 14 coupled to the outer end of the spiral Cu inductor, and a Cu wire terminal 16 coupled to the inner end of the spiral Cu inductor.

[0061] The embodiment of Figure 1 provides integration of high performance copper inductors with bond pads wherein a tall, last metal layer Cu inductor is integrated with an Al bond pad. Moreover, the tall Cu inductor can be fabricated by superposing and connecting adjacent wiring layers at the last metal and the last metal + 1, with the metal levels being interconnected by a bar via having the same shape as the metal inductor.

[0062] Figures 1a-1h illustrate the sequential steps a-h for fabrication of the first embodiment of the present invention for a spiral Cu inductor having an Al bond pad as shown in Figure 1.

[0063] Figure 1a illustrates the structure after formation of last metal layer damascene Cu interconnects in an FSG (fluoro silicate glass) dielectric using conventional processing steps of dielectric FSG deposition, trench 18 patterning,

liner 20 deposition which could be TaN or TiN, Cu deposition, and CMP (chemical mechanical polishing). The last metal layer is traditionally known as the last metal layer beneath the bond pad layer, and that terminology is maintained herein.

[0064] Figure 1b illustrates the structure after depositing two layers of Si3N4 (shown in the Figures herein as SiN) and an intermediate layer of SiO2 passivation by CVD (chemical vapor deposition), 10 to 500 nm, 200 nm preferred for each of the three layers.

[0065] Figure 1c illustrates the structure after patterning of terminal vias by lithography and RIE (reactive ion etch with a F based etch). In the present invention, a tall Cu spiral inductor is fabricated using a thick Cu layer above the chip passivation, or by interconnecting this layer and underlying wiring layers with intermediate metal bar vias having the same spiral shape as the spiral metal inductor, which is shown as the middle via 11 and the right via 13 shown in phantom which are part of one spiral bar via forming a part of the spiral inductor 10.

[0066] Figure 1d illustrates the structure after depositing multiple layers of metal for a bond pad; four successive layers from bottom to top of TaN/TiN/Al/TiN by PVD (physical

vapor deposition) or CVD, 10 to 50 nm, 50 nm preferred for TaN and TiN, 500 to 2000 nm, 1000 nm preferred for Al; depositing a Si3N4 layer by CVD, 20 to 100 nm, 50 nm preferred; patterning SiN, TiN, Al by lithography and RIE (F- and Cl- based etch); depositing Cu seed layer 30, 20 to 500 nm, 200 nm preferred by PVD.

[0067] Figure 1e illustrates the structure after depositing and patterning resist 22 for Cu inductors 10, resist thickness = 1 to 50 um; depositing Cu by electroplating to selectively form Cu in inductor regions, 1 to 50 um, 10 um preferred.

[0068] Figure 1f illustrates the structure after stripping of the resist using organic solvent or low temperature (<100C, 80C preferred), low power O2 plasma; etching Cu seed (option 1 or 2 or 3 as explained below) by sputter etch; etching TaN by RIE (F-based); selectively depositing CoWP (preferred 92% Co, 2 % W, 6% P) on Cu inductors using electroless deposition, 10 to 50 nm, 20 nm preferred; optionally depositing additional SiN passivation by CVD (optional-see Figures 7a-7f).

[0069] Figure 1g illustrates the structure after coating the substrate with polyimide 24 (1 to 50 um, 5 um preferred); forming openings to bond pads.

[0070] Figure 1h illustrates the structure after etching SiN layer on bond pads; depositing BLM (barrier layer metallurgy), such as TiW 50-500 nm, 100 nm preferred, and forming C4 solder balls. The completed tall Cu spiral inductor 10 comprises the Cu layer above the passivation 17, with a Cu via 19 forming a connection to underlying Cu wires in the last Cu metal level 15.. In a different embodiment, the tall Cu spiral inductor 10 comprises the Cu layer above the passivation 17 interconnected and superposed with underlying spiral Cu wiring layers such as last Cu metal level 15, connected with an intermediate spiral Cu bar via 19 which are all interconnected and superposed to form the tall laminate spiral Cu inductor 10 which also has an Al bond pad.

[0071] Figure 2 illustrates a top plan view of a second embodiment of the present invention for a spiral Cu inductor which is similar to the spiral Cu inductor of Figure 1 but having a Cu (copper) bond pad.

[0072] The sequential steps a-c and e-h for fabrication of the second embodiment of the present invention are substantially the same as steps a-c and e-h for fabrication of the first embodiment. Moreover, steps a-c of the second embodiment are illustrated fully in Figures 1a-1c, and ac-

cordingly the description of steps a-c is not repeated, and the description of steps d-h is given with respect to Figures 2d-2h.

[0073] Additionally, the parameters specified above for thickness and preferred thickness of the different particular layers and particular materials, exemplary compositions of alloys, examples of materials, and other specified parameters such as temperature, are equally applicable to the embodiments described below and accordingly will not be repeated in the following descriptions.

[0074] Steps a-c in the fabrication of the second embodiment are illustrated and explained with reference to Figures 1a-1c, and accordingly the explanation of the second embodiment starts with step d illustrated in Figure 2d.

[0075] Figure 2d illustrates the structure after depositing TaN barrier by PVD; depositing Cu seed layer by PVD.

[0076] Figure 2e illustrates the structure after depositing and patterning resist 40 for Cu inductors 42; depositing Cu by electroplating to selectively form Cu in inductor regions 42.

[0077] Figure 2f illustrates the structure after stripping of the resist using organic solvent or low temperature, low power O2 plasma; etching Cu seed (option 1 or 2 or 3 as ex-

plained below with reference to Figures 4-6) by sputter etch; etching TaN by RIE (F-based); selectively depositing CoWP on Cu inductors and terminals using electroless deposition; optionally depositing additional SiN passivation by CVD (see Figures 7a-7f).

[0078] The following options 1 and 2 can be employed instead of the CoWP capping layer. Options 1 and 2 are applicable to all of the embodiments herein with a CoWP capping layer.

[0079] Option 1. Other materials can be deposited by selective electroless plating instead of using CoWP, namely NiMoP, NiMoB, NiReP, NiWP.

[0080] Option 2. Use selective chemical vapor deposition (CVD) instead of selective electroless plating to deposit a passivating layer on the Cu, The preferred material is W. Other options are Mo or Ru. So for example, selective CVD W would be used instead of CoWP. The process sequence would be the same.

[0081] Figure 2g illustrates the structure after coating the substrate with polyimide 44, forming via openings 46 to bond pads.

[0082] Figure 2h illustrates the structure after depositing barrier layer metallurgy BLM (barrier layer metallurgy), and forming C4 solder balls.

[0083] Figure 3 illustrates a top plan view of a third embodiment of the present invention for a spiral Cu inductor having a raised Cu (copper) bond pad 50, Figure 3h.

[0084] The third embodiment also illustrates interconnect wiring 52 which can encompass global interconnects for cross chip wiring. The interconnect wiring could also have been illustrated in the first and second embodiments and is equally applicable to the first and second embodiments.

[0085] The sequential steps a-d and f-h for fabrication of the third embodiment of the present invention are substantially the same as steps a-d and f-h for fabrication of the second embodiment. Moreover, steps a-d of the second embodiment are illustrated fully in Figures 1a-1c and 2d, and accordingly the description of steps a-d is not repeated and the description of steps e-h is given with respect to Figures 3e-3h.

[0086] Figure 3e illustrates the structure after depositing and patterning resist 54 for raised bond pads at 50, Cu inductors at 56, and interconnect wiring at 58; depositing Cu by electroplating, selectively patterning Cu in the unmasked regions (option 1 or 2 or 3 as explained below).

[0087] Figure 3f illustrates the structure after stripping of the resist using organic solvent or low temperature O2 plasma;

etching Cu seed (option 1 or 2 or 3 as explained below) by sputter etch; etching TaN by RIE (F-based); selectively depositing CoWP on Cu inductors, terminals and interconnect wiring using electroless deposition; optionally depositing additional SiN passivation by CVD (see Figures 7a-7f).

[0088] Figure 3g illustrates the structure after coating the substrate with polyimide 60; forming via openings 62 to bond pads.

[0089] Figure 3h illustrates the structure after etching SiN, depositing BLM (barrier layer metallurgy), and forming C4 solder balls.

[0090] Figures 4, 5 and 6 illustrate respective first (1), second (2) and third (3) options for patterning Cu.

[0091] Figures 4a-4c illustrate option 1 in which the seed layer is deposited before the resist, followed by selective deposition of Cu.

[0092] Figure 4a illustrates, after the terminal via etch, the structure formed by depositing a TaN (or Ta barrier) by PVD, 10 to 100 nm(different from Figure 1d?), 50 nm preferred; depositing Cu seed layer by PVD.

[0093] Figure 4b illustrates the structure formed by depositing and patterning resist 70 for inductors, terminals and in-

terconnects; depositing Cu by electroplating, selectively forming Cu in inductor, terminal and interconnect regions.

[0094] Figures 4c illustrates the structure after stripping resist using organic solvent or low temperature, low power O2 plasma; etching Cu seed by sputter etch; etching TaN by RIE (F- based).

[0095] Figures 5a-5e illustrate option 2 in which the Cu seed layer is deposited after the resist, followed by blanket deposition of Cu and CMP.

[0096] Figure 5a illustrates, after the terminal via etch, the structure formed by depositing TaN (or Ta) barrier by PVD, 10 to 100 nm, 50nm preferred.

[0097] Figure 5b illustrates the structure formed after patterning resist for inductors, terminals and interconnects; optionally depositing Ta adhesion layer, 5 to 50 nm, 20um preferred; depositing Cu seed layer by PVD.

[0098] Figure 5c illustrates the structure after depositing Cu by electroplating.

[0099] Figure 5d illustrates the structure after removing excess Cu by CMP or electropolishing, if Ta adhesion layer was deposited, removing Ta adhesion layer by CMP (low pressure, abrasiveless CMP may be necessary to avoid damaging resist) or wet etch or dry etch.

[0100] Figure 5e illustrates the structure after stripping the resist using organic solvent or low temperature, low power O2 plasma; etching TaN by RIE (F- based).

[0101] Figures 6a-6e illustrate option 3 in which the barrier and seed layers are deposited after the resist and a blanket deposition of Ta and Cu, followed by CMP or etching.

[0102] Figure 6a illustrates the structure formed after terminal via patterning.

[0103] Figure 6b illustrates the structure formed after depositing and patterning resist for inductors, terminals and interconnects, resist thickness, 1 to 20 um; depositing a TaN adhesion layer, 5 to 50 nm, 20um preferred; depositing Cu seed layer, 20 to 500 nm, 200 um preferred, by PVD.

[0104] Figure 6c illustrates the structure after depositing Cu by electroplating, selectively forming Cu in unmasked regions.

[0105] Figure 6d illustrates the structure after removing excess Cu by CMPor electropolishing, removing TaN adhesion layer by CMP or wet etch (low pressure, abrasiveless CMP may be necessary to avoid damaging resist).

[0106] Figure 6e illustrates the structure after stripping the resist using organic solvent or low temperature, low power O2 plasma; etching TaN by RIE (F- based).

[0107] Figures 7a-7d illustrate options for passivation.

[0108] Figure 7a illustrates passivation by selective metal only; after Cu patterning and barrier etch, depositing selective passivating metal such as CoWP (10 to 100 nm) by electroless deposition.

[0109] Figure 7b illustrates passivation by dielectric depositon only; after Cu patterning and barrier etch, depositing single dielectric (100 to 500 nm Si3N4) or multilayer dielectrics (Si3N4/SiO2/Si3N4) by CVD.

[0110] Figure 7c illustrates passivation by selective metal and dielectric deposition, which is a combination of Figures 7a and 7b.

[0111] Figure 7d illustrates passivation by spacer and dielectric deposition; after Cu patterning but prior to barrier etch, deposit passivating metal or dielectric by CVD (10 to 200 nm); etchback by RIE to form spacers, also etching the barrier layer (note spacers could also be formed after barrier layer etch); deposit single layer or multilayer dielectric.

[0112] Figure 7e illustrates passivation by spacer and selective metal and dielectric deposition, which is similar to Figure 7d, but selective metal is deposited on top of Cu after spacer etches.

[0113] Figure 7f illustrates passivation by selective metal and spacer and dielectric deposition, which is similar to Figure 7d, but selective metal is deposited on Cu before spacers etch.

[0114] While several embodiments and variations of the present invention for integration of high performance copper inductors with bond pads are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.